

REMARKS

The applicant has carefully considered the official action dated September 7, 2004, and the references it cites. In the official action, claims 11-30 were allowed. Accordingly, claims 11-30 are not further discussed herein. The official action rejected claims 1-10 under 35 U.S.C. 112, second paragraph, as indefinite. In addition, Claims 1-4 were rejected under 35 U.S.C. 102(e) as anticipated by Arnold et al., U.S. Patent 6,715,060 ("Arnold et al."). By way of this response, claims 1-3 have been amended to clarify the scope of protection sought. In view of the foregoing amendments and the following remarks, the applicant respectfully requests reconsideration.

As an initial matter, the applicant wishes to address the rejections under 35 U.S.C. 112, second paragraph. Concerning claims 1-3, the official action contends that it is not clear what is meant by "updating the memory resource to prevent a data hazard." Although the applicant does not concede that it is not clear what is meant by "updating the memory resource to prevent a data hazard," claims 1-3 have been amended to recite "managing the memory resource" instead of "updating the memory resource." Support for this amendment can be found in the specification at least at: page 7, line 28 through page 8, line 5; page 9, lines 18-21; and page 12, lines 19-21. The applicant notes that no new matter has been entered, and that the foregoing amendments are not narrowing and have not been made for purposes of patentability. On the contrary, the amendments to claims 1-3 clarify and/or broaden the scope of protection sought. The applicant submits that the term "managing" may be found in other claims (e.g., claim 5) and, presumably, was clear to the examiner in those claims. Thus, the applicant believes the amendments to claims 1-3 have overcome the indefiniteness rejections of claims 1-3 and respectfully requests withdrawal of these rejections.

The official action also rejected claim 5 as indefinite. In particular, the official action contends that it is not clear what the “tracking informations” represent. However, the applicant respectfully disagrees and submits that adequate support for “tracking information” is provided in the specification, and that it would be obvious to one of ordinary skill in the art upon review of the specification that tracking information includes information that may be used to track multiple levels of pendency and the order of data returns for one or more memory registers or any other memory resource accessed by a processor (page 9, lines 15-18). Further, as described in the specification by way of example at page 9, lines 15-18, tracking information may be implemented using bits that are stored in bit fields of a data structure. Accordingly, the applicant respectfully submits that independent claim 5 and claims 6-10 dependent thereon are in condition for allowance.

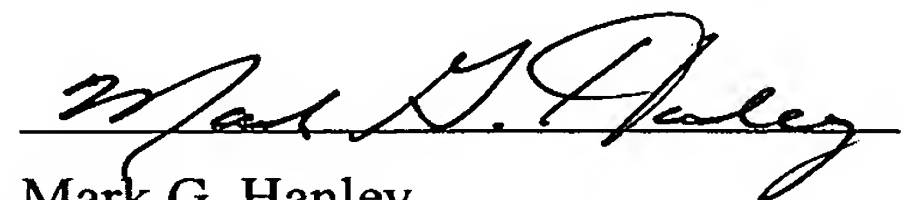
Turning to the art rejections, the applicant respectfully submits that independent claim 1 is allowable over the art of record. The official action contends that claim 1 is anticipated by Arnold et al. However, Arnold et al. fail to teach or suggest managing a memory resource to prevent a data hazard based on an order of receipt of a first instruction response and a second instruction response, as recited in independent claim 1.

The official action cites col. 2, line 59 and col. 10, line 60 to support its contention. However, the cited passages merely teach stalling or canceling one or more instructions to prevent a data hazard and do not mention or even hint at managing a memory resource to prevent a data hazard based on an order of receipt of a first instruction response and a second instruction response, as recited in claim 1. On the contrary, Arnold et al. teach managing accesses to registers based on the speculative and non-speculative nature of instructions (col. 10, lines 1-5; col. 10, lines 26-30) and the type of instruction that is pending (col. 10, lines

13-17). Specifically, Arnold et al. teach hazard detection circuitry that is configured to first determine if a pending instruction is a read instruction or a write instruction and to indicate that a retired instruction is speculative or non-speculative depending on the type (e.g., read or write) of instruction that is pending to allow or prevent canceling the retired instruction to prevent a data hazard. Thus, Arnold et al. teach managing register accesses based on instruction type and the speculative or non-speculative nature of instructions, but do not teach or suggest managing a memory resource to prevent a data hazard based on an order of receipt of a first instruction response and a second instruction response, as recited in claim 1. Accordingly, the applicant respectfully submits that independent claim 1 and claims 2-4 dependent thereon are in condition for allowance.

In view of the foregoing, the applicant respectfully submits that this application is in condition for allowance. If there are any remaining matters that the examiner would like to discuss, the examiner is invited to contact the undersigned representative at the telephone number set forth below.

Respectfully submitted,


Mark G. Hanley
Reg. No. 44,736
Attorney for Applicant
Hanley, Flight and Zimmerman, LLC
20 North Wacker Drive
Suite 4220
Chicago, Illinois 60606
312.580.1020

Dated: 12.02.04

Attorneys for Intel Corporation